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BALDRIDGE, BENJAMIN M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,092	YAKABE, MASAMI	
	Examiner	Art Unit	
	Benjamin M. Baldridge	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 -12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :3 February 2006, 21 June 2006, 19 September 2007.

DETAILED ACTION

1. Claims 1 – 12 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The abstract of the disclosure is objected to because of figure numbers included in the text of the abstract. Abstracts may be incomprehensible if the numerals of the selected figure(s) do not correspond with those in the abstract if the application is published. This should therefore be avoided. Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of numerous informalities. The specification is replete with terms and phrases which are unclear, and in some cases incomprehensible. The specification should be revised carefully to correct errors, improve clarity, and make the language of the specification consistent with proper idiomatic English. Examples of some informalities found in the specification are:

Page 1, line 29: “electricity diving into the signal wire”; the meaning of the term “diving” is unclear.

Page 2, line 1: “the conventional capacitance detection circuit 10 like this acts as follows”;

Page 2, line 24: “Here, when Vb is direct voltage”; does this mean DC voltage?

Page 3, line 15: “essential circuit”; no precise meaning can be attached to this phrase.

Page 3, line 17: “a one-tip IC”; no precise meaning can be attached to this phrase.

Appropriate correction is required.

Claim Objections

5. Claims 3, 4 and 9 are objected to because of the following informalities:

Claim 3: the meaning of the limitation “connected to a point having potential between potential of the first power supply and potential of the signal wire" is unclear. For the purposes of examination, the term "potential" will be construed to mean "voltage", consistent with the broadest reasonable interpretation of the term "potential" in this context.

Claim 4: the meaning of the limitation "pass frequency elements" is unclear. For the purposes of examination, the limitations will be construed to refer to the function of the resistance and capacitance recited in the claim, which is taken to be filtering signals as an RC filter, as either a low pass or high pass filter. Use of such filters is common in the circuit design arts, and is consistent with the broadest reasonable interpretation of the claim.

Claim 9: the meaning of the limitation “potential that is equal to or lower than potential of the first power supply and equal to or higher than potential of the second power supply" is unclear. For the purposes of examination, the term "potential" will be construed to mean "voltage", consistent with the broadest reasonable interpretation of the term "potential" in this context.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gavazzi AG (European Patent Application EP 0 723 166 A1, date of publication 24 July 1996, hereinafter referred to as Gavazzi) in view of Ker et al. (US Patent Application Publication Pub. No. US 2002/0109153 A1, Pub. Date 15 August 2002, hereinafter referred to as Gavazzi).

8. As to claim 1, Gavazzi discloses a capacitive sensor having substantial features of the claimed invention, including:

A capacitance detection circuit (P. 2, lines 34 – 35);

A first buffer amplifier unit connected to a capacitor to be detected via a signal wire (Page 2, lines 38 – 40; note that the term "signal wire" is construed to mean any wire capable of carrying a signal, including the shielded cable or wire disclosed by Gavazzi as item 7 in Figure 1);

Wherein an output terminal of the first buffer amplifier unit is connected to a first junction point of the first diode and the second diode and to a second junction point of the third diode and the fourth diode (Figure 1, items 13, 14, 15, also diodes connected to output of buffer amplifier 3, between the output of the buffer amplifier 3 and the Schmitt Trigger item 4).

Gavazzi fails to disclose:

A first diode and a second diode connected in series between the signal wire and a first power supply;

A third diode and a fourth diode connected in series between the signal wire and a second power supply.

Ker discloses:

A first diode and a second diode connected in series between the signal wire and a first power supply (Figure 10, items D1, D2, Vdd (item 1007));

A third diode and a fourth diode connected in series between the signal wire and a second power supply (Figure 10, items D3, D4, Vss (item 1008).

Given the teaching of Ker, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi by employing well known or conventional features such as a first and second diode and third and fourth diode connected in series between a signal wire and first and second power supplies, as disclosed by Walton, in order to reduce parasitic capacitances on the signal wire, and thereby improve the noise immunity of the sensor.

As to claim 2, Gavazzi discloses:

Wherein the voltage gain of the first buffer amplifier unit is 1 (Page 2, lines 38 - 40; note that Gavazzi explicitly discloses unity gain of a buffer amplifier, and discusses the voltage output; note also that the use of unity gain buffer amplifiers to furnish a high input impedance and low output impedance is common in the circuit and sensor design arts. The use of such amplifiers is well known to persons of ordinary skill in those arts, and would have been an obvious to such persons at the time of the invention as a means to increase the sensitivity of the capacitive sensor).

As to claim 9, Gavazzi discloses:

A circuit that detects capacitance of a capacitor to be detected (P. 2, lines 34 – 35; note that the term “capacitor to be detected” is construed as an object to be detected by the capacitive sensor; such an interpretation is consistent with the specification).

Wherein an output terminal of the buffer amplifier unit is connected to a junction point of the first diode and the second diode and to a junction point of the third

diode and the fourth diode (Figure 1, items 13, 14, 15, also diodes connected to output of buffer amplifier 3, between the output of the buffer amplifier 3 and the Schmitt Trigger item 4).

Gavazzi fails to disclose:

A first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes;

A third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that current flows from the second power supply to the signal wire via the third and fourth diodes;

A resistor connected between the signal wire and potential that is equal to or lower than the potential of the first power supply and equal to or higher than the potential of the second power supply.

Ker discloses:

A first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes (Figure 10, items D1, D2, Vdd (item 1007); note that current may flow from the wire to Vdd if the voltage on the wire is greater than Vdd);

A third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that current flows from the second power supply to the signal wire via the third and fourth diodes (Figure 10, items D3, D4, Vss (item 1008); note that current may flow from the second power supply to the signal wire via the diodes if the voltage on the wire is less than Vss);

A resistor connected between the signal wire and potential that is equal to or lower than the potential of the first power supply and equal to or higher than the potential of the second power supply (Figure 10, note connection of item 2 back to common point of item 15. Note also that limitation **"potential that is equal to or lower than the potential of the first power supply and equal to or higher than the potential of the second power supply"** is construed to mean a voltage level somewhere between Vdd and Vss as shown in Figure 10).

Given the teaching of Ker, a person of ordinary skill in the art would have readily

recognized the desirability and advantages of modifying the capacitive sensor of

Gavazzi by employing well known or conventional features such as a first and second diode and third and fourth diode connected in series between a signal wire and first and second power supplies, and a resistor connected to the signal wire, as disclosed by Ker, in order to reduce parasitic capacitances on the signal wire, and thereby improve the noise immunity of the sensor.

9. Claims 3, 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gavazzi in view of Ker, as applied to claims 1, 2 and 9 above, and further in view of Landt (US Patent 5,285,120, February 8, 1994, hereinafter referred to as Landt).

As to claim 10, Gavazzi in view of Ker disclose an apparatus as discussed in paragraph 9 above. Specifically, Gavazzi in view of Ker discloses an apparatus including:

A circuit that detects capacitance of a capacitor to be detected (Gavazzi, P. 2, lines 34 – 35; note that the term "capacitor to be detected" is construed as an object to be detected by the capacitive sensor; such an interpretation is consistent with the specification);

A buffer amplifier unit connected to the capacitor to be detected via a signal wire and of which the voltage gain is 1 (Gavazzi, Page 2, lines 38 – 40; note that the term "signal wire" is construed to mean any wire capable of carrying a signal, including the shielded cable or wire disclosed by Gavazzi as item 7 in Figure 1. See also comments regarding unity gain of buffer amplifiers in discussion of claim 2, above);

A first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes (Ker, Figure 10, items D1, D2, Vdd (item 1007); note that current may flow from the wire to Vdd if the voltage on the wire is greater than Vdd);

A third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that current flows from the second power supply to the signal wire via the third and fourth diodes (Ker, Figure 10, items D3, D4, Vss (item 1008); note that current may flow from the second power supply to the signal wire via the diodes if the voltage on the wire is less than Vss);

A resistor connected between (i) potential that is equal to or lower than potential of the first power supply and equal to or higher than potential of the second power supply and (ii) the signal wire (Ker, Figure 10 - note connection of item 2 back to common point of item 15. Note also that limitation "**potential that is equal to or lower than the potential of the first power supply and equal to or higher than the potential of the second power supply"** is construed to mean a voltage level somewhere between Vdd and Vss as shown in Figure 10);

A resistor connected to the first junction point and to a point having potential between potential of the first power supply and potential of the signal wire (Ker, Figure 10, items 1007 (Vdd), 1008 (Vss), R; note connection to connection point 1002 in Figure 10);

A resistor connected to the second junction point and to a point having potential between potential of the second power supply and potential of the signal wire (Ker, Figure 10, items 1007 (Vdd), 1008 (Vss), R; note connection to connection point 1002 in Figure 10. Note also that use of a second resistor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Gavazzi in view of Ker fails to disclose:

A capacitor connected between an output terminal of the buffer amplifier unit and a first junction point of the first diode and the second diode;

A capacitor connected between the output terminal of the buffer amplifier unit and a second junction point of the third and fourth diode.

Landt discloses:

A capacitor connected between an output terminal of the buffer amplifier unit and a first junction point of the first diode and the second diode (Column 2, lines 30 – 32. Note that the use of a capacitor as a DC block, or to couple AC signals, is a common practice in the circuit design arts, and would have been obvious to a person of ordinary skill in that art as a routine exercise of ordinary skill, and necessary to prevent unwanted DC bias on the diode junction due to possible voltage offset in the buffer amplifier).

A capacitor connected between the output terminal of the buffer amplifier unit and a second junction point of the third and fourth diode (Column 2, lines 30 – 32. Note that the use of a capacitor as a DC block, or to couple AC signals, is a common practice in the circuit design arts, as discussed immediately above. Note also that use of

a second capacitor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*);

Given the teaching of Landt, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker by employing well known or conventional features such as a first and second coupling capacitor between the output of the buffer amplifier and junction of the diodes, as disclosed by Landt, in order to block DC currents due to DC voltage offset in the buffer amplifier, and thereby prevent unwanted biasing (and capacitance due to varactor effects) of the diodes.

As to claim 3, Gavazzi in view of Ker discloses:

The first junction is connected to a point having potential between potential of the first power supply and potential of the signal wire via a first resistor (Figure 10, item 1007 (Vdd), 1008 (Vss), R; note connection to point 1002. Note also discussion of interpretation of the term "potential" in paragraphs 6 and 9 above);

The second junction point is connected to a point having potential between potential of the second power supply and potential of the signal wire via a second resistor (Ker, Figure 10, items 1007 (Vdd), 1008 (Vss), R; note connection to connection point 1002 in Figure 10. Note also that use of a second resistor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Gavazzi in view of Ker fails to disclose:

The output terminal of the first buffer amplifier unit is connected to a first junction point via a first capacitance and to a second junction point via a second capacitance.

Landt discloses:

The output terminal of the first buffer amplifier unit is connected to a first junction point via a first capacitance and to a second junction point via a second capacitance (Column 2, lines 30 – 32. Note that the use of a capacitor as a DC block, or to couple AC signals, is a common practice in the circuit design arts, as discussed above. Note also that use of a second capacitor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Given the teaching of Landt, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker by employing well known or conventional features such as a first and second capacitance between the output of the buffer amplifier and junction of the diodes, as disclosed by Landt, in order to block DC currents due to DC voltage offset in the buffer amplifier, and thereby prevent unwanted biasing (and capacitance due to varactor effects) of the diodes.

As to claim 4, Gavazzi in view of Ker fail to disclose:

The first resistor and the first capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected and AC component of biased voltage added to said capacitor to be detected;

The second resistor and second capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected and AC component of biased voltage added to said capacitor to be detected.

Landt discloses:

The first resistor and the first capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be

detected and AC component of biased voltage added to said capacitor to be detected (Column 2, lines 30 – 32; note explicit disclosure of RC filter (i.e. resistor – capacitor) used to select desired frequency components or passband and reject unwanted or out of band signals);

The second resistor and second capacitor are, respectively, a resistance value and a capacitance value that pass frequency elements of output signals from the first buffer amplifier unit corresponding to variant capacitance of the capacitor to be detected and AC component of biased voltage added to said capacitor to be detected (Column 2, lines 30 – 32; note explicit disclosure of RC filter (i.e. resistor – capacitor) used to select desired frequency components or passband and reject unwanted or out of band signals. Note also that use of a second RC filter, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Given the teaching of Landt, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker by employing well known or conventional features such as a first and second RC filter between the output of the buffer amplifier and junction of the diodes, as disclosed by Landt, in order to pass desired signal components and reject unwanted out of band signal components, thereby improving the noise performance of the capacitive sensor.

10. Claims 5, 6, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gavazzi in view of Ker and in view of Landt, as applied to claims 3, 4, and 10 above, and further in view of Enriquez et al. (US Patent 6,950,514 B2, September 27, 2005, hereinafter referred to as Enriquez).

As to claim 5, Gavazzi in view of Ker and in view of Landt disclose an apparatus as discussed in paragraph 10 above.

Gavazzi in view of Ker and in view of Landt fail to disclose:

A second buffer amplifier unit connected between (i) a junction point of the first resistor and first capacitor and (ii) the first junction point;

A third buffer amplifier unit connected between (i) a junction point of the second resistor and the second capacitor and (ii) the second junction point.

Enriquez discloses:

A second buffer amplifier unit connected between (i) a junction point of the first resistor and first capacitor and (ii) the first junction point (Column 3, lines 31 – 35; Column 4, lines 10 - 12; note that Enriquez explicitly discloses the use of buffer amplifiers to minimize loading of a high pass resistor - capacitor (RC) filter. Note also that the use of buffer amplifiers to present a high impedance to a sensor or isolate circuit components from loading effects is a common practice in the sensor design arts, and would have been obvious to a person of ordinary skill in the art at the time of the invention);

A third buffer amplifier unit connected between (i) a junction point of the second resistor and the second capacitor and (ii) the second junction point (Column 3, lines 31 – 35; Column 4, lines 10 - 12; note that Enriquez explicitly discloses the use of buffer amplifiers to minimize loading of a high pass resistor - capacitor (RC) filter; note also that repeated use of a buffer amplifier configured as recited in the instant limitation constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Given the teaching of Enriquez, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker and in view of Landt by employing well known or conventional features such as a second and third buffer amplifier, as disclosed by Enriquez, in order to isolate the resistor/capacitor combination from loading effects, thereby improving the sensitivity of the capacitive sensor.

As to claim 6, Gavazzi in view of Ker and in view of Landt discloses:

Each voltage gain of the first to third buffer amplifier units is set so that the potential of the first junction point and the potential of the second junction point are the same as potential of the signal wire (Gavazzi, Figure 1, item 3. Note that

unity gain buffer amplifiers, as disclosed by Gavazzi, will achieve the potentials recited in the instant claim. Note also that repeated use of a buffer amplifier configured as recited in the instant limitation constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

As to claim 11, Gavazzi in view of Ker and in view of Landt discloses:

A circuit that detects capacitance of a capacitor to be detected (Gavazzi, P. 2, lines 34 – 35; note that the term "capacitor to be detected" is construed as an object to be detected by the capacitive sensor; such an interpretation is consistent with the specification);

A first buffer amplifier unit connected to the capacitor to be detected via a signal wire and of which voltage gain is 1 (Gavazzi, Page 2, lines 38 – 40; note that the term "signal wire" is construed to mean any wire capable of carrying a signal, including the shielded cable or wire disclosed by Gavazzi as item 7 in Figure 1. Note also that Gavazzi explicitly discloses unity gain of a buffer amplifier, and discusses the voltage output; note also that the use of unity gain buffer amplifiers to furnish a high input impedance and low output impedance is common in the circuit and sensor design arts. The use of such amplifiers is well known to persons of ordinary skill in those arts, and would have been an obvious to such persons at the time of the invention as a means to increase the sensitivity of the capacitive sensor);

A first diode and a second diode connected in series between the signal wire and a first power supply in a way that a current flows from the signal wire to the first power supply via the first and second diodes (Figure 10, items D1, D2, Vdd (item 1007); note polarity of diodes);

A third diode and a fourth diode connected in series between the signal wire and a second power supply in a way that a current flows from the second power supply to the signal wire via the third and fourth diodes (Figure 10, items D3, D4, Vss (item 1007); note polarity of diodes);

A first resistor connected to a junction point of the first capacitor and the second buffer amplifier unit and to a point having potential between potential of the first power supply and potential of the signal wire (Ker, Figure 10 - note connection of item 2 back to common point of item 15. Note also that limitation **"potential that is equal to or lower than the potential of the first power supply and equal to or higher than the potential of the second power supply"** is construed to mean a voltage level somewhere between Vdd and Vss as shown in Figure 10);

A second resistor connected to a junction point of the second capacitor and the

third buffer amplifier unit and to a point having potential between potential of the second power supply and potential of the signal wire; (Ker, Figure 10, items 1007 (Vdd), 1008 (Vss), R; note connection to connection point 1002 in Figure 10. Note also that use of a second resistor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*);

A third resistor connected between (i) potential that is equal to or lower than potential of the first power supply and equal to or higher than potential of the second power supply and (ii) the signal wire (Ker, Figure 10, items 1007 (Vdd), 1008 (Vss), R; note connection to connection point 1002 in Figure 10. Note also that use of a third resistor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*);

A first capacitor and **a second capacitor** (Landt, Column 2, lines 30 – 32. Note that the use of a capacitor as a DC block, or to couple AC signals, is a common practice in the circuit design arts, as discussed above. Note also that use of a second capacitor, connected as recited in this limitation, constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Gavazzi in view of Ker and in view of Landt fail to disclose:

A second buffer amplifier unit connected in series between an output terminal of the first buffer amplifier unit and a first junction point of the first diode and the second diode;

A third buffer amplifier unit connected in series between the output terminal of the first buffer amplifier unit and a second junction point of the third diode and fourth diode.

Enriquez discloses:

A second buffer amplifier unit connected in series between an output terminal of the first buffer amplifier unit and a first junction point of the first diode and the second diode (Column 3, lines 31 – 35; Column 4, lines 10 - 12; note that Enriquez explicitly discloses the use of buffer amplifiers to minimize loading of a high pass resistor - capacitor (RC) filter. Note also that the use of buffer amplifiers to present a

high impedance to a sensor or isolate circuit components from loading effects is a common practice in the sensor design arts, and would have been obvious to a person of ordinary skill in the art at the time of the invention);

A third buffer amplifier unit connected in series between the output terminal of the first buffer amplifier unit and a second junction point of the third diode and fourth diode (Column 3, lines 31 – 35; Column 4, lines 10 - 12; note that Enriquez explicitly discloses the use of buffer amplifiers to minimize loading of a high pass resistor - capacitor (RC) filter; note also that repeated use of a buffer amplifier configured as recited in the instant limitation constitutes duplication of parts, and as such would have been obvious to one having ordinary skill in the art at the time the invention was made. It has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193 USPQ 8*).

Given the teaching of Enriquez, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker and in view of Landt by employing well known or conventional features such as a second and third buffer amplifier, as disclosed by Enriquez, in order to present the diode junctions with a low output impedance, thereby improving the sensitivity of the capacitive sensor.

As to claim 12, the method disclosed in the instant claim is intrinsic to the circuit disclosed in claim 11, as discussed above, since the method steps will be met during the normal operation of the system stated above.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gavazzi in view of Ker, as applied to claims 1, 2, and 9 above, and further in view of Fong (US Patent 6,005,439, December 21, 1999, hereinafter referred to as Fong) and further in view of Zandman et al. (US Patent 6,441,475 B2, August 27, 2002, hereinafter referred to as Zandman).

As to claim 7, Gavazzi in view of Ker disclose an apparatus as discussed in paragraph 9 above.

Gavazzi in view of Ker fail to disclose:

The first buffer amplifier includes a MOSFET as an input circuit;

A gate of the MOSFET is connected to an input terminal of the first buffer amplifier unit.

Fong discloses:

The first buffer amplifier includes a MOSFET as an input circuit (Figures 1 and 2, disclosed as prior art, clearly showing a MOSFET used as an input device. The use of MOSFETs is a common practice among persons of ordinary skill in the circuit design arts, wherever a high input impedance is required);

A gate of the MOSFET is connected to an input terminal of the first buffer amplifier unit (Column 3, lines 51 – 55).

Given the teaching of Fong, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker by employing well known or conventional features such as a MOSFET as an input circuit, in common source or drain configuration, so as to use the gate of the MOSFET as an input, as disclosed by Fong, in order to present a high input impedance to a capacitive sensor, thereby improving the overall sensitivity of the sensor.

Gavazzi in view of Ker and in view of Fong fail to disclose:

A substrate of the MOSFET is connected to an output terminal of the first buffer amplifier unit.

Zandman discloses:

A substrate of the MOSFET is connected to an output terminal of the first buffer amplifier unit (Column 1, lines 37 – 40, cited as prior art; also Column 3, lines 1 - 6.

Note that the drain (i.e. substrate) of the device is typically on the backside of the device, and that use of a MOSFET in common source configuration (as shown in Fong, Figures 1 and 2) would require the substrate as an output).

Given the teaching of Zandman, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker and in view of Fong employing well known or conventional features such as a MOSFET substrate connected to an output terminal of a buffer amplifier unit, as disclosed by Zandman, in order to present a high input impedance to a capacitive sensor, thereby improving the overall sensitivity of the sensor.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gavazzi in view of Ker, as applied to claim 1, 2 and 9 above, and further in view of Taylor (US Patent Application Publication Pub. No. US 2002/0074988 A1, Pub. Date June 20, 2002, hereinafter referred to as Taylor).

As to claim 8, Gavazzi in view of Ker disclose an apparatus as discussed in paragraph 9 above.

Gavazzi in view of Ker fail to disclose:

A testing terminal for an input of a testing signal;

A testing capacitor and a switch connected in series between the input terminal of the first buffer amplifier unit and the testing terminal.

Taylor discloses:

A testing terminal for an input of a testing signal ([0019], lines 1 – 3);

A testing capacitor and a switch connected in series between the input terminal of the first buffer amplifier unit and the testing terminal ([0020], lines 1 – 10).

Given the teaching of Taylor, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the capacitive sensor of Gavazzi in view of Ker by employing well known or conventional features such as a testing terminal for inputting a test signal, and a test capacitor and switch, as disclosed by Taylor, in order to allow users to test the capacitive sensor offline and while in use.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin M. Baldridge whose telephone number is 571 270 1476. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571 272 2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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